Abstract

A timer circuit is arranged for reduced propagation delay and improved stability at low supply voltages. The timer circuit includes a capacitor circuit, a voltage offset circuit, an inverter circuit, and a current source circuit. The current source circuit is arranged to provide a current. Also, the capacitor circuit is arranged to provide a voltage ramp in response to the current. The voltage offset circuit is configured to provide a voltage offset. Further, the current source circuit, the capacitor circuit, and the voltage offset current are arranged to provide two voltage ramps that are offset from each other. Additionally, the inverter circuit includes a p-type transistor and an n-type transistor. The p-type transistor is configured to receive one of the two voltage ramps, and the n-type transistor is configured to receive the other of the two voltage ramps.